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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,122	05/08/2001	Martin Czech	Micronas.6158	4157
7590	11/02/2004		EXAMINER	
Patrick J O'Shea Esq Samuels Gauthier & Stevens LLP 225 Franklin Street Suite 3300 Boston, MA 02110			RICHARDS, N DREW	
			ART UNIT	PAPER NUMBER
			2815	
			DATE MAILED: 11/02/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/852,122	CZECH ET AL.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 04 August 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-8 and 13-18 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-8 and 13-18 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 08 May 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-8 and 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 lines 11-13 recites "said first region being separated from said second region by a distance that corresponds to a dimension of the gate electrode." This limitation is indefinite as one cannot ascertain what distance is being claimed. The distance is claimed to "correspond" to a dimension of the gate electrode but the claim does not specify how it corresponds. For example, the distance could be a 1 to 1 correspondence to a dimension of the gate electrode. It could also be a 2 to 1, 3 to 1, 1.5 to 1 correspondence, or any other set ratio defining the two lengths.

Claim 2-8 are similarly rejected as they contain the same limitations of independent claim 1 from which they depend.

Claim 16 lines 17 and 18 recites a similar limitation with regard to an insulator dimension and the distance between the first and second regions. Claim 16 is indefinite in a similar manner to claim 1. Claims 17 and 18 are similarly rejected as they contain the same limitations of independent claim 16 from which they depend.

Claim 18 is further indefinite as it depends from itself. It appears that it should depend from claim 17 and will be treated as such for the sake of the art rejections below.

3. Insofar as definite, the claims are rejected over prior art as follows.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Voldman et al. (U. S. Patent No. 6,015,993).

Voldman et al. disclose an ESD protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential and a second potential bus with a second supply potential, the electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region 142 doped with a first conduction type P and a second region 144 spaced apart from the first region 142, the second region doped a second conduction type N (figure 5);

wherein the electrostatic discharge protective structure is located between the first 232 and second potential busses 234 and drains off an overvoltage pulse to one of the first and second potential busses (figure 12A); and

wherein the laterally formed electrostatic discharge diode includes a gate electrode 136,140 located between the first region 142 and the second region 144, the first region being separate from the second region by a distance that corresponds to a dimension of the gate. In this case, figure 4 shows the distance between the first and second region corresponding to the width of the gate plus two sidewall spacers and figure 5 shows the distance between the first and second region corresponding to the width of the gate plus one sidewall spacer.

With regard to claim 2, the protective structure includes a semiconductor body 122 having a surface in which the first and second regions are embedded (figure 5), wherein the first region is connected via a first electrode to the first potential bus and the second region is connected via a second electrode to the second potential bus (figure 12A). Though the first and second electrode are not explicitly shown, they are nonetheless implicitly disclosed as figure 12A shows the first and second regions (anode and cathode) connected to the busses and one would necessarily have electrodes to provide such connection.

With regard to claim 3, the semiconductor body 122 includes charge carriers of the second conduction type N and the gate electrode and second electrode are connected to the second potential bus (figure 12A, col. 5 line 66 through col. 6 line 13).

With regard to claim 4, the semiconductor body is substrate 124 which includes charge carriers of the first conduction type, and at least one well 122 of the second conduction type is embedded in the semiconductor body 124, the first and second regions 142,144 are embedded in the well 122 (figure 5).

With regard to claim 6, the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit (col. 2 lines 12-13, the ESD protection is for a MOSFET circuit).

With regard to claim 7, Voldman et al. further disclose a gate dielectric 130 that spaces the semiconductor body at a distance from the gate electrode (figure 5).

With regard to claim 8, the gate dielectric contains silicon dioxide and the gate electrode contains polysilicon.

6. Claims 1-3, 6-8 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun et al. (U.S. Patent No. 6,344,385 B1).

Jun et al. disclose an ESD protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential and a second potential bus with a second supply potential, the electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region 13 doped with a first conduction type N and a second region 36 spaced apart from the first region 13, the second region doped a second conduction type P (figure 3a);

wherein the electrostatic discharge protective structure is located between the first 34 and second potential busses (ground) and drains off an overvoltage pulse to one of the first and second potential busses (figure 3a); and

wherein the laterally formed electrostatic discharge diode includes a gate electrode 35 located between the first region 13 and the second region 36, the first region being separate from the second region by a distance that corresponds to a dimension of the gate (figure 3a).

With regard to claim 2, the protective structure includes a semiconductor body 11 having a surface in which the first and second regions are embedded (figure 3a), wherein the first region is connected via a first electrode to the first potential bus and the second region is connected via a second electrode to the second potential bus (figure 3a).

With regard to claim 3, the semiconductor body 11 includes charge carriers of the second conduction type P and the gate electrode and second electrode are connected to the second potential bus (figure 3a).

With regard to claim 6, the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit (figure 3a, the circuit protects the MOS transistor form from source and drain 31 and 32 and gate 33).

With regard to claim 7, Jun et al. further disclose a gate dielectric that spaces the semiconductor body at a distance from the gate electrode (figure 3a).

With regard to claim 8, the gate dielectric contains silicon dioxide and the gate electrode contains polysilicon. The gate 35 is formed the same as the gate 33 of the MOS transistor, and thus discloses the same polysilicon gate and silicon dioxide gate dielectric (col. 3 line 12-35).

With regard to claim 13, Jun et al. disclose an integrated circuit with electrostatic discharge protection comprising:

a circuit (MOS transistor formed by 31,32,33) to be protected (figure 3a);

an electronic discharge device 28 that is disposed electrically parallel to the circuit to be protected between first 34 and second (ground) voltage busses, wherein the electrostatic discharge device includes a laterally shaped electrostatic discharge diode having:

a first region 13 doped with a first conduction type material P within a substrate 11 (figure 3a);

a second region 36 doped with a second conduction type material P within the substrate (figure 3a); and

a gate electrode 35 having a width W and located between the first 13 and second 36 regions such that the first and second regions are separated by the width W (figure 3a).

With regard to claim 14, Jun et al. further disclose a gate oxide disposed on the substrate between the first and second conduction regions and underlying the gate

electrode (figure 3a, the gate is disclosed as MOS gate, thus containing an oxide between the gate and the substrate).

With regard to claim 15, Jun et al. do not explicitly disclose an first electrode on the substrate overlying the first region or a second electrode overlying the substrate in the second region. However, Jun et al. do disclose the first region being connected to the first voltage bus and the second region being connected to the second bus. In showing the electrical connection from the substrate to the busses, Jun et al. is implicitly disclosing electrodes to form the connections. One would recognize that electrodes would inherently be formed to provide the electrical connection.

#### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman et al. (U.S. Patent No. 6015993) as applied to claims 1-4 and 6-8 above, and further in view of Williams (U.S. Patent No. 6,060,752).

Voldman et al. teach all the limitations of claim 4, from which claim 5 depends. However, Voldman et al. do not teach the second region laterally enclosing the first region.

Williams teach an electrostatic discharge device including diodes. Williams teach in figure 11A-G various configurations of the first (P) and second (N) regions where the second region laterally encloses the first region.

Voldman et al. and Williams are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the second region to laterally enclose the first region. The motivation for doing so is to provide improved carrier confinement. Therefore, it would have been obvious to combine Voldman et al. with Williams to obtain the invention of claim 5.

9. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (U.S. Patent No. 6,344,385 B1) in view of Voldman et al. (U.S. Patent No. 6015993).

With regard to claim 16, Jun et al. disclose an integrated circuit with electrostatic discharge protection comprising:

a circuit (MOS transistor formed by 31,32,33) to be protected (figure 3a);

an electronic discharge device 28 that is disposed electrically parallel to the circuit to be protected between first 34 and second (ground) voltage busses, wherein the electrostatic discharge device includes a laterally shaped electrostatic discharge diode having:

a first region 13 doped with a first conduction type material P within a substrate 11 (figure 3a);

a second region 36 doped with a second conduction type material P within the substrate (figure 3a);

an insulator (not shown, but the gate is disclosed as a MOS gate, thus containing an oxide between the gate and the substrate) between the gate 35 and the substrate 11 and thus between the first and second electrodes; and

a gate electrode 35 (figure 3a).

Jun et al. do not explicitly disclose a first electrode in communication with the first region or a second electrode in communication with the second region. However, Jun et al. do disclose the first region being connected to the first voltage bus and the second region being connected to the second bus. In showing the electrical connection from the substrate to the busses, Jun et al. is implicitly disclosing electrodes to form the connections. One would recognize that electrodes would inherently be formed to provide the electrical connection.

Jun et al. do not teach the insulator (gate oxide) having an insulator dimension that corresponds to the distance between the first and second regions. It is noted that the gate 35 is the same length as the distance between the first and second regions.

Voldman et al. teaches a similar integrated circuit with electrostatic discharge protection. Voldman et al. teach in figure 1A, 1B, 2, 4, 5, 6 and 7, an insulator formed between the gate and the substrate (for example, insulator 108 in figure 1A) that is formed to the same length as the gate. It is well known in the art to form the gate insulator to the same pattern as the gate as shown in Voldman et al. This structure is common in the art because it results from the use of a single patterning step to pattern

the entire gate structure (gate and insulator) so as to save on production steps, time, and cost by eliminating the need for a separate etch for the gate and the insulator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the insulator of Jun et al. to the same dimension as the gate as shown in Voldman et al. in order to simplify processing to obtain the invention of claim 16.

With regard to claim 17, the insulator includes an oxide.

With regard to claim 18, the oxide is not specifically disclosed as silicon dioxide. However, Voldman et al. teach growing the oxide on the surface of a silicon substrate. One of ordinary skill in the art at the time of the invention would recognize that a grown silicon oxide layer would be silicon dioxide.

#### ***Response to Arguments***

10. Applicant's arguments filed 8/4/04 have been fully considered but they are not persuasive.

First, applicant argues that Voldman et al.'s gate electrode does not have a dimension that corresponds to the distance between the first and second regions. This is not persuasive. Even though the gate may not have the exact same dimension as the distance between the first and second regions, it still has a dimension that "corresponds". The claim language does not require the dimensions to be equal or have a 1 to 1 correspondence and thus Voldman et al. still reads on the invention as claimed.

Second, applicant argues that Jun et al. do not teach two doped regions separated by a distance that corresponds to the dimension of a gate electrode therebetween. Applicant seems to be arguing that 33 is the only gate electrode in the structure and that layer 35 is not a gate electrode. This is not persuasive as layer 35, though referred to as a controllable dummy poly silicon layer, layer 35 is considered to be the exact same structurally as a gate electrode. It is spaced apart from the substrate by an insulator and controls the current flow between two doped regions. Thus, layer 35 is considered a gate electrode and Jun et al. does teach two doped regions (13,36) separated by a distance that corresponds to the dimension of a gate electrode (35) therebetween.

Applicant also argues that none of the references teach an insulator that is in contact with the gate electrode. This is not persuasive. Voldman et al. clearly shows an oxide (insulator) 130 in figures 4-7 that is in contact with the gate electrode. Jun et al. does not show their insulator, but they disclose the gate being a MOS gate. It is known in the art that MOS is short for "Metal Oxide Semiconductor". Thus inherently including an insulator (oxide) contacting the gate (metal).

### ***Conclusion***

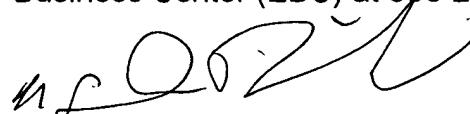
11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

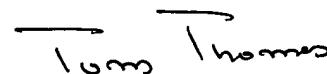
Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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